AM2827S Three Phase Brushless Motor Driver

Features

- 2.7V to 13.5V Operating Voltage Range
- 5A Maximum Drive Current
- Wide PWM input operating range to 100KHz
- Low MOSFET ON-resistance: HS + LS 80mΩ
- Built-in precise LDO Regulator 3.3V ±3%
- Operating ambient junction temperature: -20℃~85℃
- Turbo current limit function adjusts by external Resistor.
- Over temperature protection
- QFN6 X 6 Package for small PCB layout
- Halogen-Free Green Product & RoHS compliant Package

Application

- Gimbal
- Robotics
- Consumer products
- Household appliance
- For 1~2 cells batteries source application.

Description

The AM2827S provides three individual controllable half-bridge drivers. The device is intended to drive a three-phase brushless DC motor, though it can also be used to drive solenoids or other types of load. Each output driver channel consists of P-channel +N-channel power MOSFETs in a half-bridge configuration.

The AM2827S can supply up to 10A peak or 5A RMS output current per channel (with proper PCB heat sink at 10V and 25℃) per half-Bridge. There is internal shutdown function for over-temperature protection.

The device provides internal shutdown functions for Short-circuit protection, turbo current limit and over temperature protection.

Ordering Information

Part number	Package	Body Size
AM2827S	QFN 6X6	6.0mm X 6.0mm

● Absolute Maximum Ratings (T_A=25℃)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	PVCC_X	19	V
Analog- Supply Voltage	VCC	19	V
Output Continuous Current	Io_{CONT}	5	A
Output Peak Current	Io_{peak}	10	A
Operate Temperature Range	T_{opr}	-20～+85	℃
Storage Temperature Range	T_{stg}	-40～+150	℃

● Recommended Operating Conditions (T_A =25℃)

(Set the power supply voltage taking allowable dissipation into considering)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	PVCC_X	2.7(Note)	10	13.5	V
Analog- Supply Voltage	VCC	2.7(Note)	10	13.5	V
PWM_X and STBY_X	V_{PWM_X} / V_{STBY_X}	-0.3	3.3	3.7	V
H-bridge Output Continuous Current	I_{OUT}			5	A
Externally Applied PWM Frequency	F_{PWM}	0.02		100	KHz

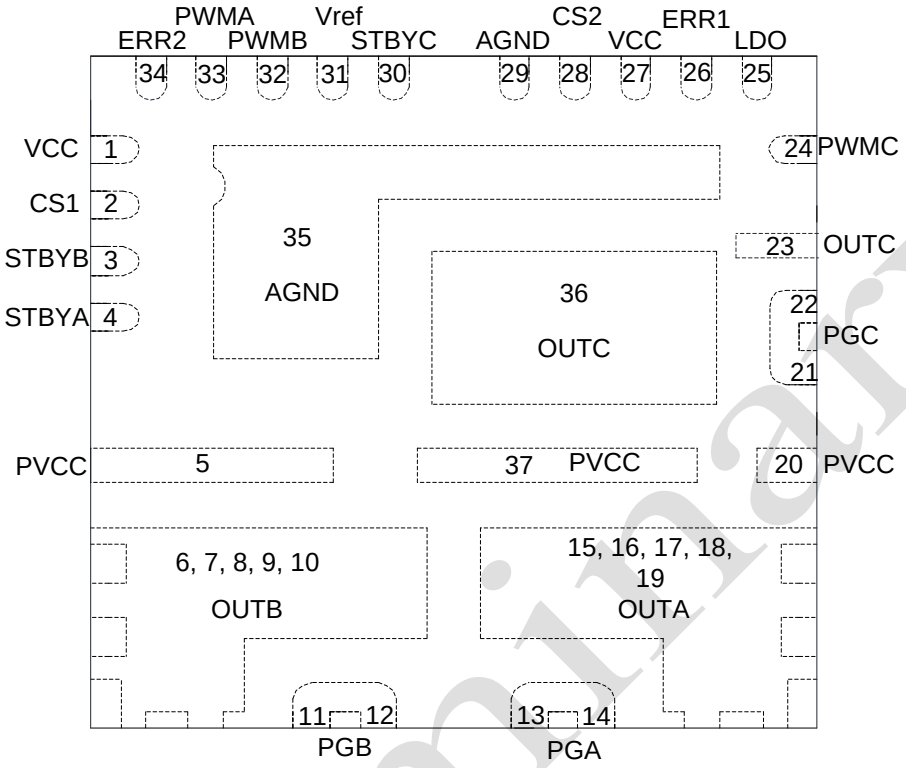
Note:

1. The LDO_3.3V operation range should be considered in choosing VCC.
2. The LDO 3.3V operation range should be considered in choosing VCC and LDO voltage drop 0.4V max at ILDO=100mA.

- **Electrical Characteristics (Unless otherwise specified, TA = 25℃,PVCC=VCC=10V)**

Parameter	Symbol	Value			Unit	Condition
		MIN	TYP	MAX		
Power Supply						
VCC/PVCC Operating Current1	I_{CC1}		0.5		mA	PWM_X=STBY_X=L
VCC/PVCC Operating Current2	I_{CC2}		1		mA	PWM_X=STBY_X=H
LDO						
Output Voltage	V_{LDO}	3.2	3.3	3.4	V	I_{LDO}=100mA, VCC=10V
Dropout Voltage	V_{DO}	—	—	400	mV	I_{LDO}=100mA, V_{LDO}=3.3V
PWM_X/STBY_X Inputs						
Input High Level Logic	V_{PWM_XH} V_{STBY_XH}	2.0		3.5	V	
Input Low Level Logic	V_{PWM_XL} V_{STBY_XL}	0		0.7	V	
Input Frequency	F_{PWM}	0.02		100	kHz	
Input Pull-up Resistance	R_{IPD}		100		KΩ	
Input Pull-down Resistance	R_{IPD}		130		KΩ	
H-bridge FETs						
Rds(on) HS+LS FET on-resistance	$R_{ds(on)}$		55		mΩ	I_{Load} = 1A, T_J: 25℃
Current Sense Input						
Current Sense Voltage	V_{CS}	120	150	180	mV	

- **Pin configuration QFN 6X6**

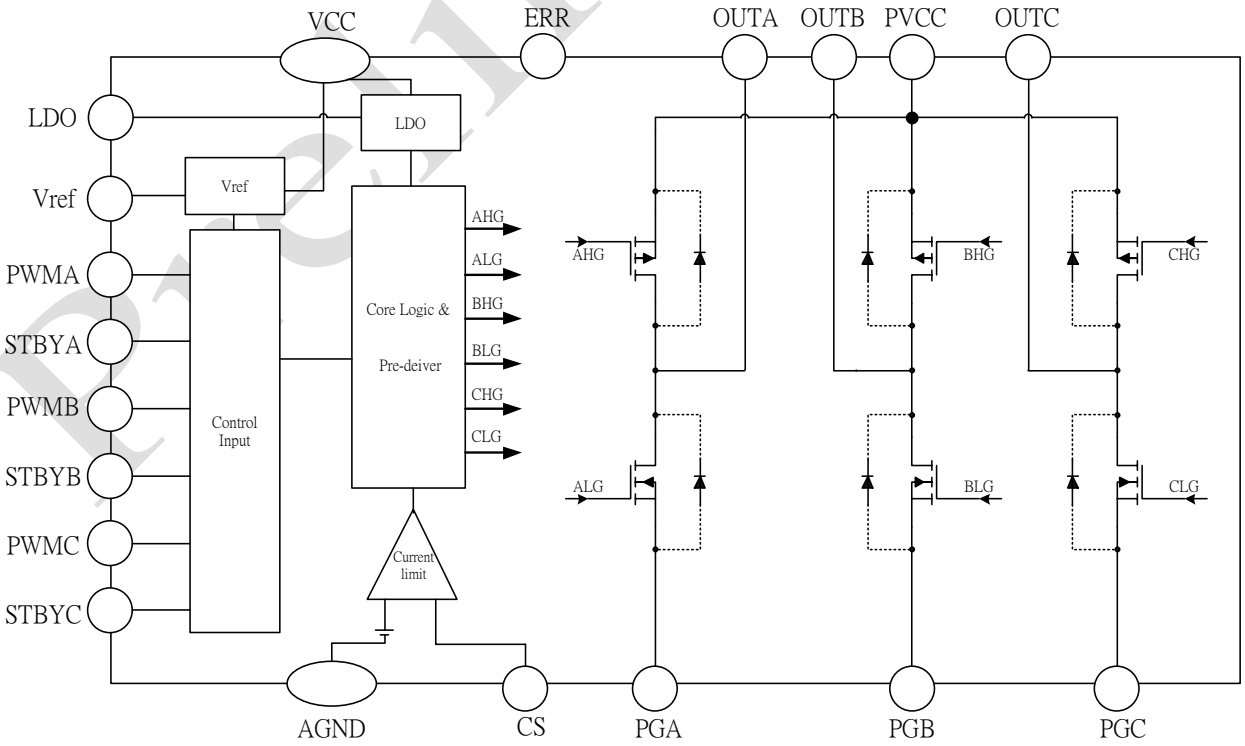


- **Pin Descriptions**

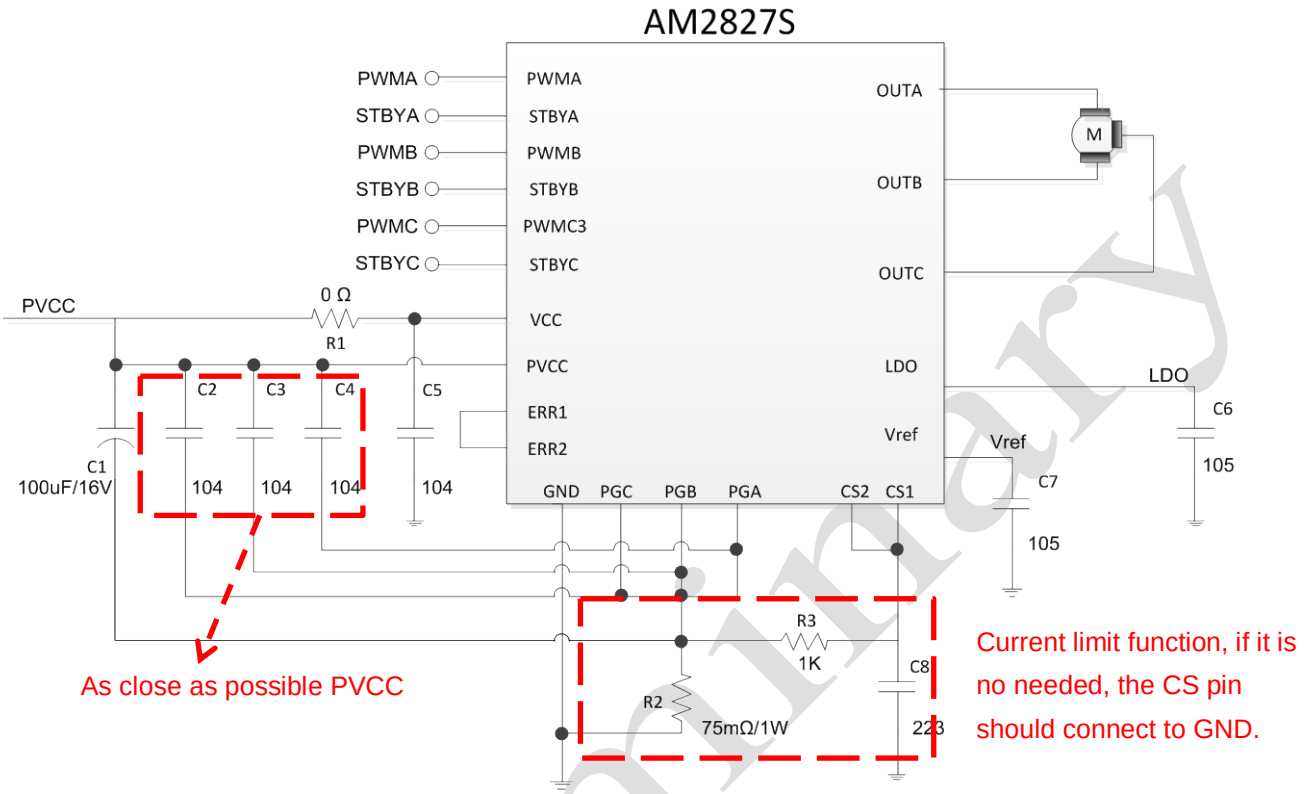
PIN Number	Pin Name	I/O	Description
1, 27	VCC	-	Analog Power Supply
2	CS1	I	Current Sense 1
3	STBYB	I	Standby Input B
4	STBYA	I	Standby Input A
5, 20, 37	PVCC	-	Power Supply of Half Bridge
6, 7, 8, 9, 10	OUTB	O	Output of Half Bridge B
11, 12	PGB	-	Power GND of Half Bridge B
13, 14	PGA	-	Power GND of Half Bridge A
15, 16, 17, 18, 19	OUTA	O	Output of Half Bridge A
21, 22	PGC	-	Power GND of Half Bridge C

23, 36	OUTC	O	Output of Half Bridge C
24	PWMC	I	Driver Logic Input C
25	LDO	O	Low Dropout Regulator
26	ERR1	I	Error Output 1
28	CS2	I	Current Sense 2
29, 35	AGND	-	Analog Ground
30	STBYC	I	Standby Input C
31	Vref	O	Internal Reference Voltage
32	PWMB	I	Driver Logic Input B
33	PWMA	I	Driver Logic Input A
34	ERR2	I	Error Output 2

● Block Diagram



Application Circuit



Description:

1. The C1、C2、C3、C4 are power supply stabilization for both PWM driver and kickback absorption. A large capacitor C1 must be used when the coil inductance is large or when coil resistance is low. The pattern connecting to PVCC and GND must be as wide and as short as possible.
2. The C5 is analog power supply stabilization. The pattern connecting to VCC and GND must be as short as possible.
3. AM2827S Vref and LDO output are for internal reference voltage using, the Vref and LDO output should be always turn on, C6 and C7 capacitor must be connect to GND.
4. R2 is a current sense resistor. R3 and C8 as a low pass filter to catch the voltage of R2 for current sense function. If the current sense function is not needed then short PGA, PGB, PGC, CS1 and CS2 PIN to GND
5. ERR1 PIN and ERR2 PIN should be connected to each other which can provide an error massage to MCU.

Application Note

1) **PVCC Capacitor：**

The PVCC capacitor is power supply stabilization for both PWM driver and kickback absorption. Normally PVCC Capacitor is 47~100uF. The pattern connecting to PVCC and GND must be as wide and as short as possible

2) **VCC Capacitor：**

The VCC capacitor is power supply stabilization. Low pass filter is composed of R and C can be used to suppress PWM driver noise and kickback absorption. Normally R=0ohm, C=0.1uF. The pattern connecting to VCC and GND must be as short as possible**.**

3) **LDO Capacitor：**

Recommend Capacitor=1μF or more.

4) **CS1/CS2**：

CS1/CS2 is current limit input pin. There is a reference voltage (150mV_TYP) at input node A of comparator. The input node B of comparator is CS1/CS2. When input voltage of CS1/CS2 >150mV, that will trigger current limit function to keep output current on setting value.

5) **ERR1/ERR2**：

ERR1/ERR2 is an error message output pin. ERR1 PIN and ERR2 PIN should be connected to each other which can provide an error message to MCU. Error message signal includes TSD function.

When IC is operating normally, ERR1/ERR2 keep high level signal, When IC is operating abnormally, ERR1/ERR2 pull low level signal which feedback to MCU.

6) **Setting Current limiter design target**：

The current limiter value is calculated in equation

$$I_{LIMITED} = \frac{150mV}{R_{SENSE}}$$

For example:

If design target for current limiter is 4.5A, the R_{SENSE} value may be calculated as following:

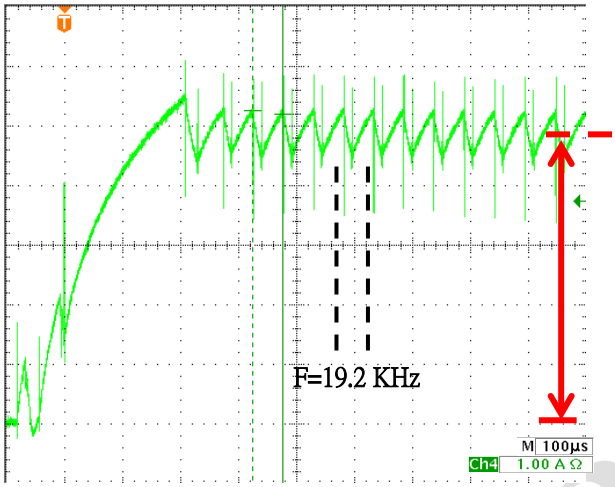
$$R_{SENSE} = \frac{150mV}{I_{LIMITED}} = \frac{150mV}{4.5A} \cong 33m\Omega$$

Please follow steps to set up R_{SENSE} value in real application circuit

Step 1. Initial setting R3=1KΩ, then calculate R_{SENSE}：

EX1 : If current limit setting $I_{LIMITED}$ 4A； $R_{SENSE} = \frac{150mV}{I_{LIMITED}} \Rightarrow \frac{150mV}{4A} = 37.5m\Omega$ ，

Initial value R_{SENSE} =37.5mΩ、R3=1KΩ、C8=100nF, the motor output waveform is as follows：

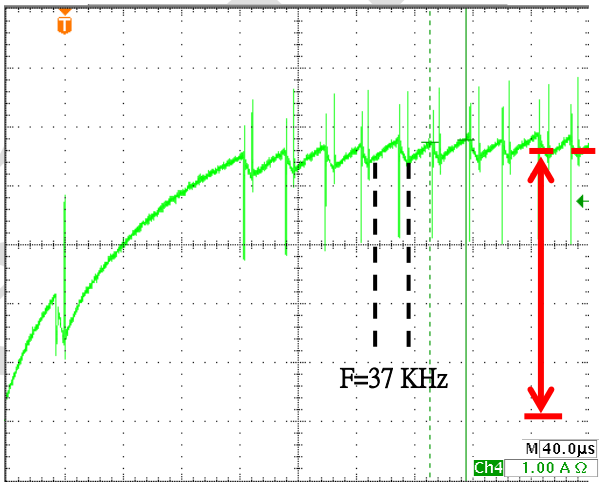


Test Condition：
VCC=6V, STBYA=STBYB=PWMA=DC 3V, PWMB=DC 0V, R3=1KΩ、C8=100nF、R_{LIMIT}=37.5mΩ

There are different type motors which have different inductive reactance and resistance, customers have to follow real motor load status to optimize R_{SENSE} limit value; therefore, please follow step 2、step 3 to optimize C8 and R_{SENSE} value again.

Step 2. Optimize C8 to make motor output working frequency in 30~40KHz range：

EX2：Change C8 from100nF to 22nF, R3=1KΩ (R_{SENSE} =37.5mΩ) stays the same, the output current waveform is as follows：



Test Condition：
VCC=6V, STBYA=STBYB=PWMA=DC 3V, PWMB=DC 0V, R3=1K、C8=22nF、R_{LIMIT}=37.5mΩ

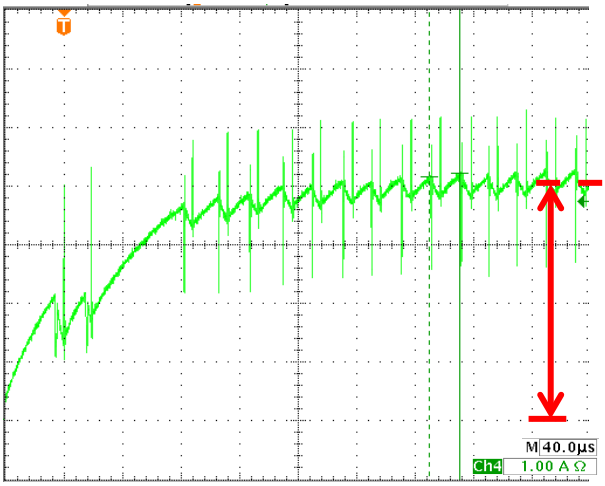
Result：The output frequency is in 30~40 KHz range after C8 value is changed.

Note 2：After C8 value is optimized for different type motor load, the current limit clamp level is shifted, customers have to follow step 3 to optimize R_{SENSE} value to obtain correct current limit clamp level.

Step 3. Optimize R_{SENSE}：

Base on step 2 output waveform result, please optimize R_{SENSE} value again to obtain correct current limit clamp level $I_{LIMITED}$.

EX3：Fix R3, C8 value, optimize R_{SENSE} from 37.5 mΩ to 50mΩ, the output current waveform is as follows：



Test Condition：
VCC=6V, STBYA=STBYB=PWMA=DC 3V, PWMB=DC 0V, R3=1KΩ、C8=22nF、R_{LIMIT}=50mΩ

The final setting value are R_{SENSE} =50mΩ、R3=1KΩ、C8=22nF, the Current Limit = 4.0A which meets customer application current limit level.

Note1：When using the same R_{SENSE} and R3 and C8, the current limit clamp level might be different because the different type motor (inductive reactance and resistance might be different) and different VCC value. To get the best current limit clamp level, it needs to test in actual load model when motor type and VCC setting is changed,

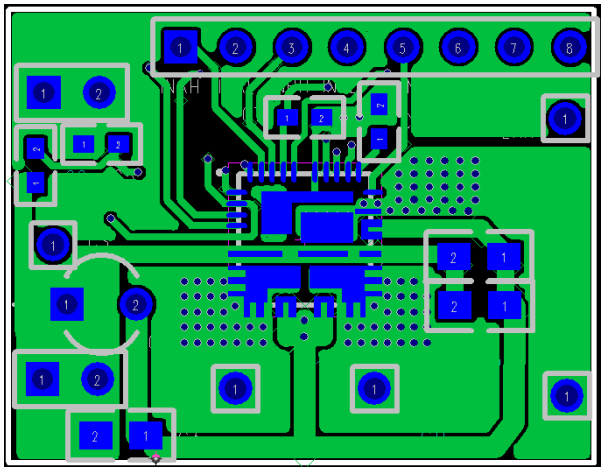
Note 2：If current limit function is not needed, the CS pins should be connected directly to ground.

7) Over-temperature protection：
If the IC junction temperature exceeds 150°C (Typ.), the internal over-temperature protection function will be triggered, partial FETs in the H-bridge are disabled, that will ensure the safety of customers' products. If the IC junction temperature falls to 110°C(Typ.), the IC resumes automatically.

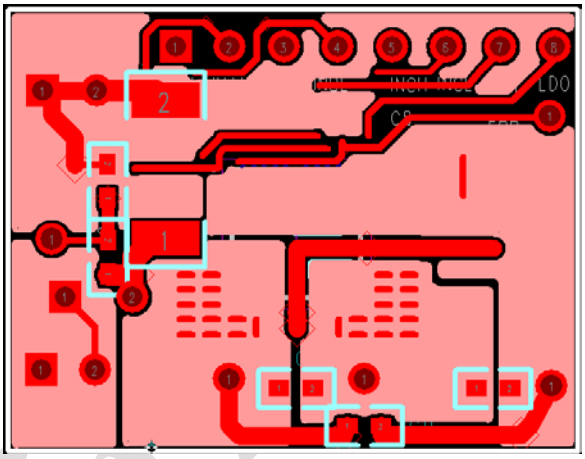
Layout Guidelines

1. Layout Example

   PCB Size 26.7x20.7 mm^2 、double side



Top Layer



Bottom Layer

2. Layout Consideration

   The layout is very important when designing high current and high frequency switching converters. Layout will affect noise pickup. Correctly layout can realize a good design with less background noise.

   Make all the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of GND planes and polygons for power distribution and heat dissipation.

   Capacitor connected at three output terminals should be as close to AM2827S as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them.

   The Power QFN is a thermally enhanced package. Based on thermal performance, it is recommended to use at least a two-layers PCB. To effectively remove heat from the device, the exposed pad should be connected to the output plane using vias. Layout example illustrates the implementation of the layout guidelines outlined above, on the AM2827S two-layer demo board.

3. Power trace

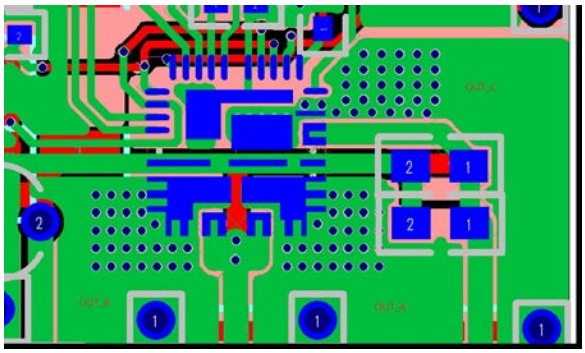
   3.1 Power trace (PVCC) should be as short as possible.

   3.2 On the PCB configuration, the C1 、C2、C3、C4 must be mounted as close as possible to PVCC pin, in order to reduce EMI noise.

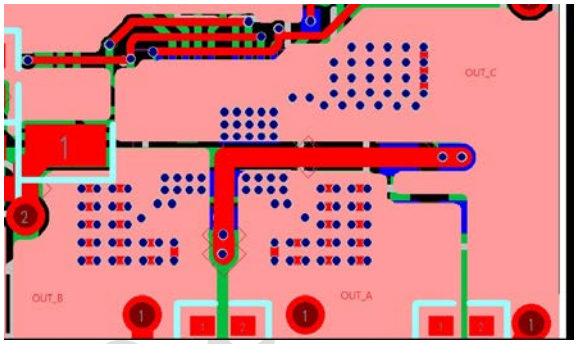
4. OUTPUT

4.1 For OUT_A & OUT_B & OUT_C PCB design consideration, multiple vias should be used to connect to a large bottom-layer & large top-layer.

4.2 For OUT_A & OUT_B & OUT_C thermal design consideration, keep the thermal pad connection as large as possible, both on the bottom side and top side. It should be big one piece of copper without any gaps.



TOP layer

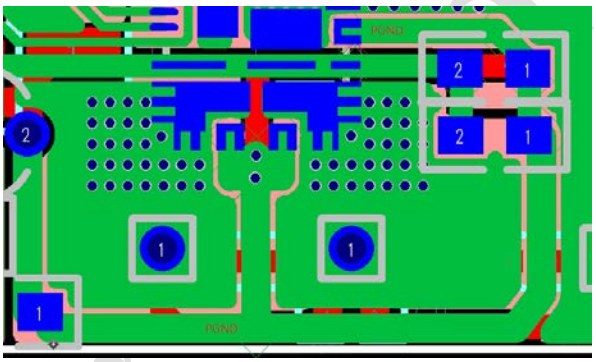


Bottom layer

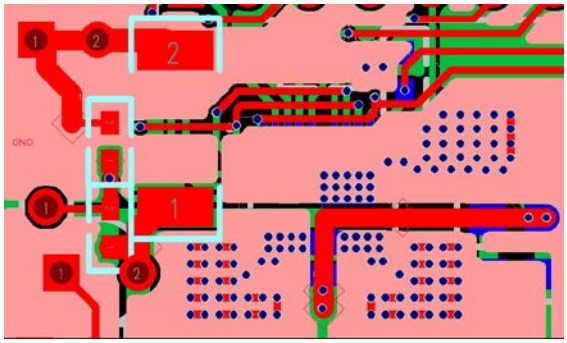
5. PGND

5.1 PGND (PG_A & PG_B &PG_C) is high-current path through the motor driver. The width of connecting metal trace should be as wide as possible.

5.2 When using the current limit function, R_{SENSE} should be as closed to AM2827S GND as possible.



TOP layer

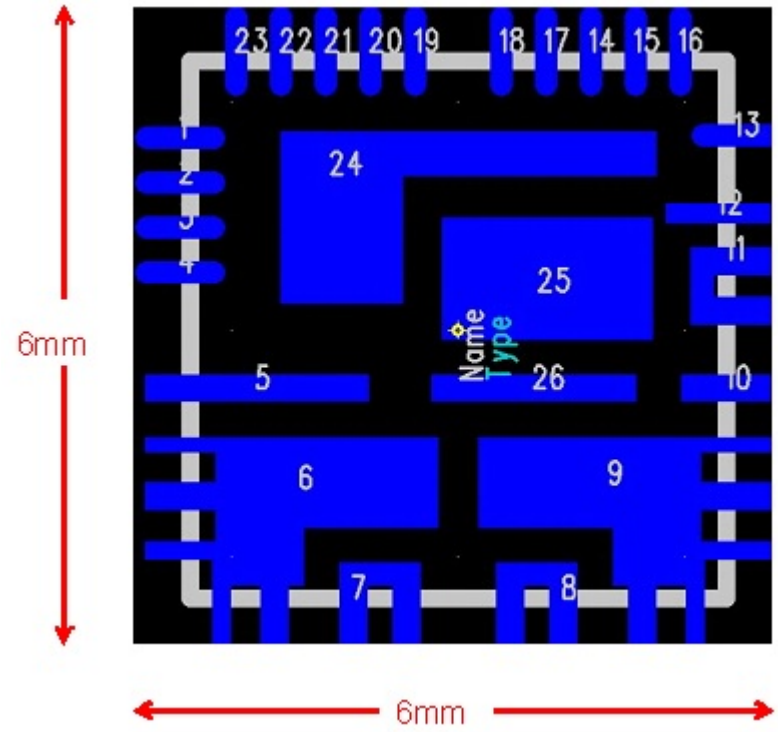


Bottom layer

6. CS Pin

6.1 The C11 capacitor should be as closer to R2 GND as possible.

7. Thermal pad PCB Via hole layout



7.1 The IC Bottom layer pad should be bigger than top layer thermal pad.

7.2 When solder paste prints on PCB, Bottom pad do not print solder paste on it.

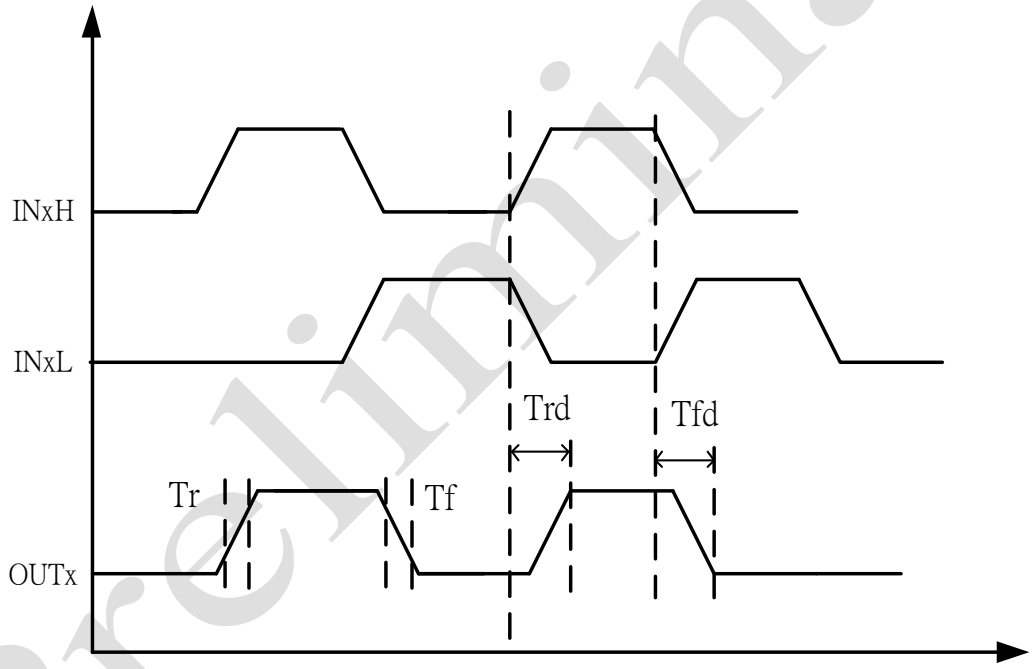
7.3 We suggest via holes diameter should be designed around 0.3mm in order to let solder paste wick down via. It can help to transfer heat to PCB.

7.4 Via hole should be as more as possible to cover whole pad. That will be useful to dissipate heat

8. Remarks: PCB top layer pad: When stencil design, solder paste do not print on all pad to avoid IC solder short.

Timing Requirement

Timing parameter	Parameter	Typical value	Unit	Condition
Output rising time	T_r	30	ns	T_A = 25℃ , VCC =PVCC=10 V , F_{IN_x}=10 kHz ,R_{load}=20 Ω
Output falling time	T_f	70	ns	
Output rising delay time	T_{rd}	600	ns	
Output falling delay time	T_{fd}	350	ns	



1) T_r : Output rising time, output voltage rising from 10% to 90%.
2) T_f : Output falling time, output voltage falling from 90% to 10%..
3) T_{rd} : Delay time, INxH/INxL low to OUTx high.
4) T_{fd} : Delay, time, INxH/INxL high to OUTx Low.

Truth Table

The PWM_X and STBY_X pins control the state (high or low) of the OUT_X outputs. Table1. Shows the logic:

STBY_X	PWM_X	OUT_X
0	X	Hi-Z
1	0	L
1	1	H

Table1. Logic States

Note:

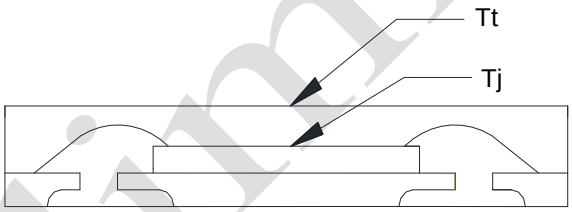
Z：High impedance

Thermal Information

θja	junction-to-ambient thermal resistance	37℃/W
Ψjt	junction-to-top characterization parameter	0.8℃/W

- **Θja** is obtained in a simulation on a JEDEC-standard 2s2p board as specified inJESD-51.
- The **Θja** number listed above gives an estimate of how much temperature rise is expected if the device was mounted on a standard JEDEC board.
- When mounted on the actual PCB, the **Θja** value of JEDEC board is totally different than the **Θja** value of actual PCB.
- **Ψjt** is extracted from the simulation data to obtain **Θja** using a procedure described in JESD-51, which estimates the junction temperature of a device in an actual PCB.

- The thermal characterization parameter, **Ψjt**, is proportional to the temperature difference between the top of the package and the junction temperature. Hence, it is useful value for an engineer verifying device temperature in an actual PCB environment as described in JEDEC JESD-51-12.
- When Greek letters are not available, **Ψjt** is written Psi-jt.
- Definition:



$$\text{DFEINITION } \Psi_{jt} = (T_j - T_t) / P_d$$

Where :

Ψjt (Psi-jt) = Junction-to-Top(of the package) °C/W
Tj= Die Junction Temp. °C
Tt= Top of package Temp at center. °C
Pd= Power dissipation. Watts

- Practically, most of the device heat goes into the PCB, there is a very low heat flow through top of the package, So the temperature difference between **Tj** and **Tt** shall be small, that is any error caused by PCB variation is small.

- This constant represents that **Ψjt** is completely PCB independent and could be used to predict the **Tj** in the environment of the actual PCB if **Tt** is measured properly.

- **How to predict Tj in the environment of the actual PCB**

Step 1 : Used the simulated **Ψjt** value listed above.

Step 2 : Measure **Tt** value by using

- **Thermocouple Method**

  We recommend use of a small ~40 gauge(3.15mil diameter) thermocouple. The bead and thermocouples wires should touch the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be heat-insulated to prevent cooling of the bead due to heat loss into wires. This is important towards preventing “too cool” **Tt** measurements, which would lead to the calculated **Tj** also being too cool.

- **IR Spot Method**

  An IR Spot method should be utilized only when using a tool with a small enough spot area to acquire the true top center “hot spot”.
  Many so-called “small spot size” tools still have a measurement area of 0~100+mils at “zero” distance of the tool from the surface. This spot area is too big for many smaller packages and likely would result in cooler readings than the small thermocouple method.
  Consequently, to match between spot area and package surface size is important while measuring **Tt** with IR sport method.

Step 3 : calculating power dissipation by

$$P \cong (VCC - \left| V_{0\_Hi} - V_{0\_Lo} \right|) \times I_{out} + VCC \times Icc$$

Step 4 : Estimate **Tj** value by

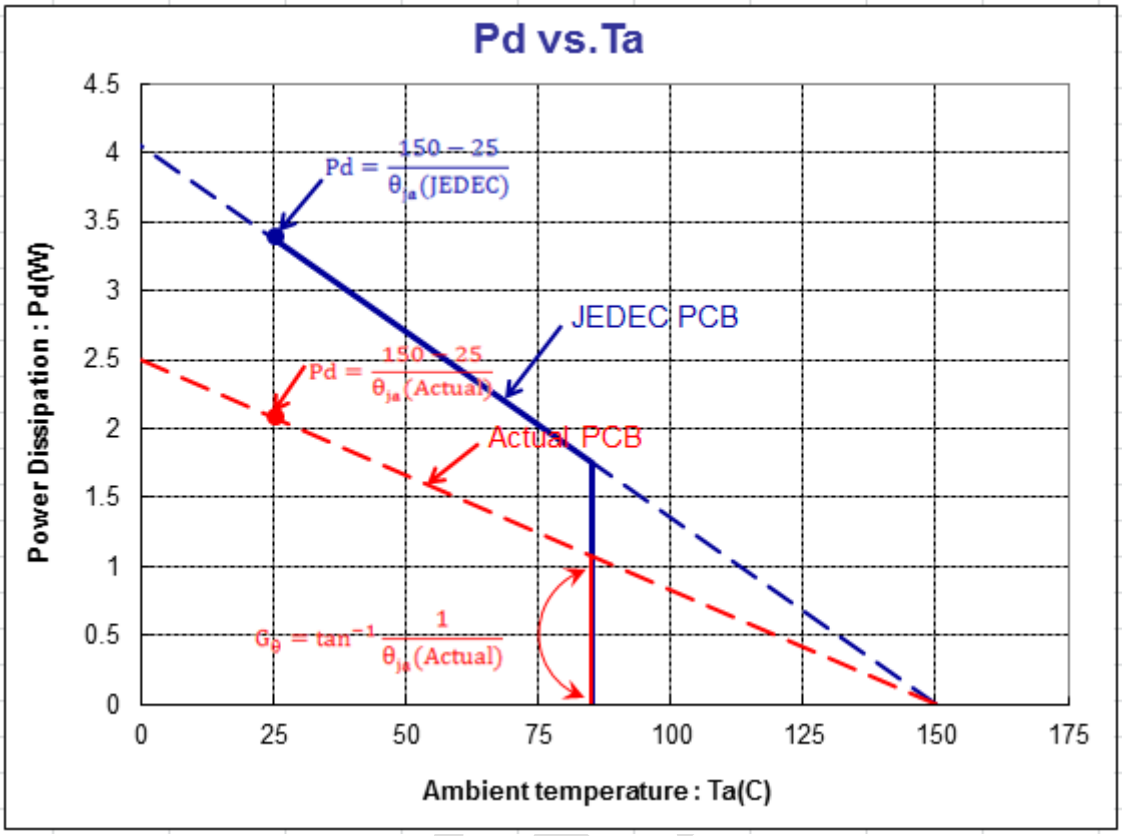
$$Tj = \Psi\mathrm{jt} \times P + Tt$$

Step 5: Calculated Θja value of actual PCB by the known **Tj**

$$\Theta\mathrm{ja}_{(\mathrm{actual})} = \left(Tj - Ta\right) / \mathrm{P}$$

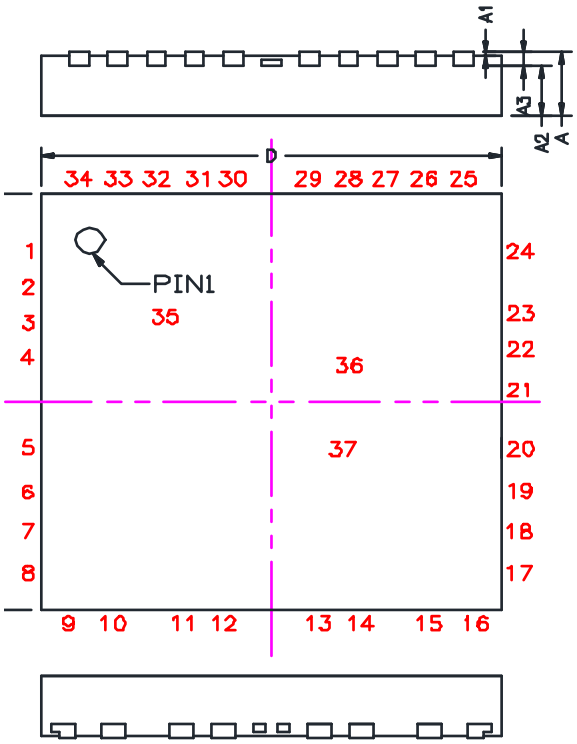
Maximum Power Dissipation (de-rating curve) under JEDEC PCB & actual PCB

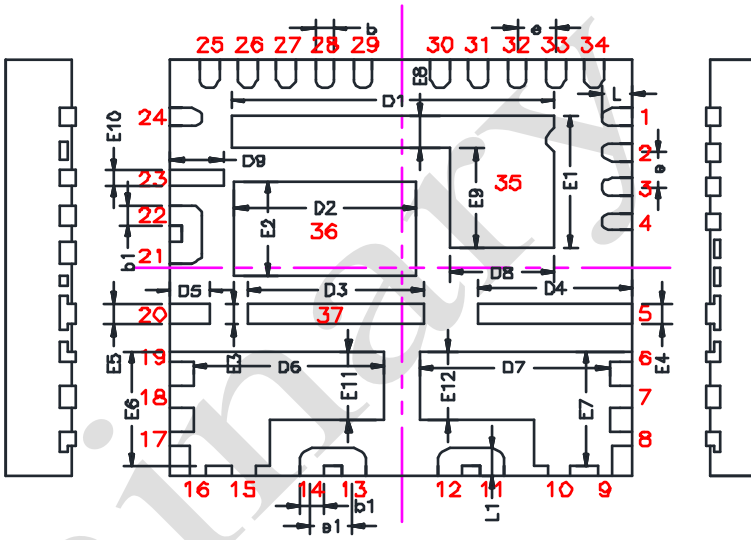
- **Power dissipation curve:**

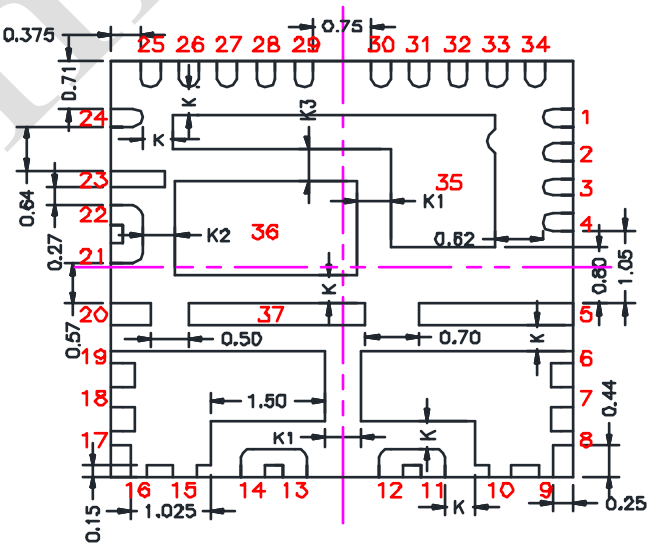


Actual PCB Based on 40x40 mm^2 FR4 PCB (1 oz.) at double side PCB

● **Package outline--- QFN 6x6** **Unit :mm**





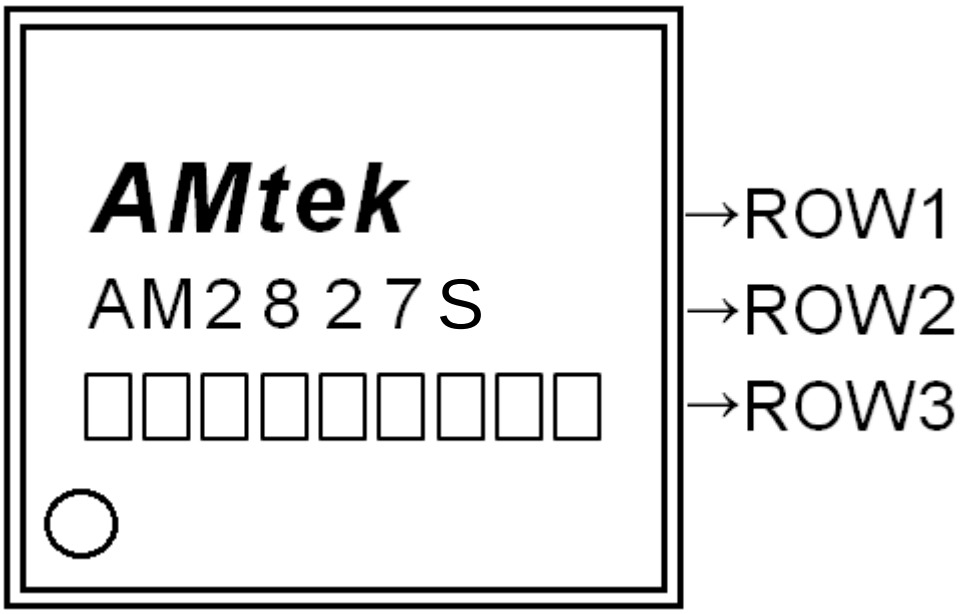


SYMBOL	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	--	0.05	0.000	--	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.203 REF			0.008 REF		
D	5.90	6.00	6.10	0.232	0.236	0.240
E	5.90	6.00	6.10	0.232	0.236	0.240
D1	4.13	4.18	4.23	0.163	0.165	0.167
D2	2.30	2.35	2.40	0.091	0.093	0.094
D3	2.25	2.30	2.35	0.089	0.091	0.093
D4	1.95	2.00	2.05	0.077	0.079	0.081
D5	0.45	0.50	0.55	0.018	0.020	0.022
D6/D7	2.425	2.475	2.525	0.095	0.097	0.099
D8	1.302	1.352	1.402	0.051	0.053	0.055
D9	0.628	0.678	0.728	0.025	0.027	0.029
E1	1.858	1.908	1.958	0.073	0.075	0.077
E2	1.308	1.358	1.408	0.051	0.053	0.055
E3/E4/E5	0.25	0.30	0.35	0.010	0.012	0.014
E6/E7	1.592	1.642	1.692	0.063	0.065	0.067
E8	0.428	0.478	0.528	0.017	0.019	0.021
E9	1.38	1.43	1.48	0.054	0.056	0.058
E10	0.17	0.22	0.27	0.007	0.009	0.011
E11/E12	0.942	0.992	1.042	0.037	0.039	0.041
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.25	0.30	0.35	0.010	0.012	0.014
L/L1	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 BSC			0.020 BSC		
e1	0.55 BSC			0.022 BSC		
K	0.40 BSC			0.016 BSC		
K1	0.45 BSC			0.018 BSC		
K2	0.43 BSC			0.017 BSC		
K3	0.472 BSC			0.019 BSC		

- **Marking Identification**

.Package Type : QFN 6X6

.Device：AM2827S

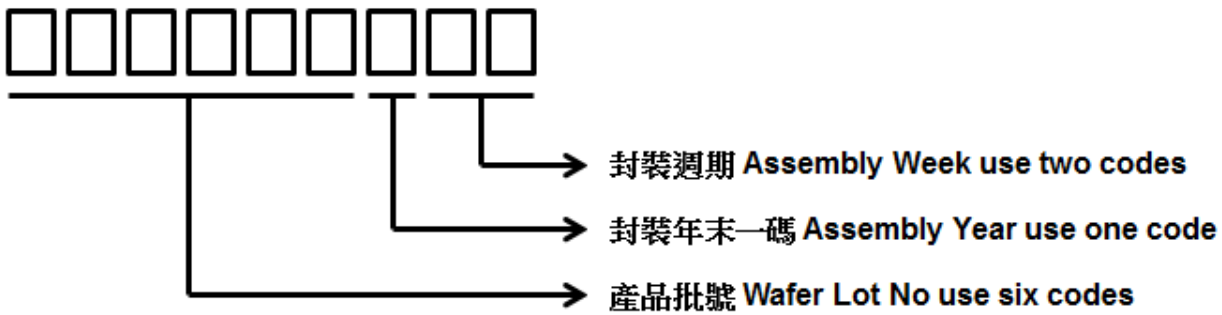


NOTE:

說明一 **Row1** ：公司名稱 **Logo**

說明二 **Row2** ：產品型號 **Device Name**

說明三 **Row3** ：產品批號 **Wafer Lot No use six codes**、封裝年末一碼 **Assembly Year use one code**、封裝週期 **Assembly Week use two codes**



Example: Wafer lot no is GD8888 + Year 2015 is F + Week 08 is 08，we type 〝GD8888F08〞

The last code of assembly year, explanation as below:：

(Year： A=0,B=1,C=2,D=3,E=4,F=5,G=6,H=7,I=8,J=9. For example: year 2015=F)